IN THE UNITED STATES DISTRICT COURT
FOR THE MIDDLE DISTRICT OF NORTH CAROLINA

THE TRUSTEES OF PURDUE UNIVERSITY,	)	
Plaintiff,	)	
v.	)	1:21-cv-840
WOLFSPEED, INC.,	)	
Defendant.	)	

ORDER FOR SUPPLEMENTAL BRIEFING

This court has separately addressed claim construction of terms in U.S. Patent No. 7,498,633 ("the '633 Patent"). On May 5, 2023, this court held a claim construction hearing with the parties — Plaintiff, the Trustees of Purdue University, and Defendant, Wolfspeed, Inc. — at which time this court took the matter under advisement. (Minute Entry 05/05/2023.) During briefing and the claim construction hearing, Defendant raised a concern about the '633 Patent's guidance, or lack thereof, concerning where the JFET region's width is measured. This court will now request supplemental briefing on this discrete issue as it pertains to the following claim terms. For conciseness and clarity, this court will use "A,", "B," and "C" as follows to specify the particular claim terms being discussed within this Order.

Claim ID (within this Order)	Claim Term	Plaintiff's Construction	Defendant's Construction
A	"a JFET region defined between the first source region and the second source region" (Claim 9)	No construction necessary	Indefinite
B	"the JFET region having a width less than about three micrometers" (Claim 9)	No construction necessary	Indefinite
C	"the JFET region having a width of about one micrometer" (Claim 10, depends from Claim 9)	No construction necessary	Indefinite

In addition to the arguments addressed by the court in its Claim Construction Memorandum Opinion and Order, Defendant argues that the '633 Patent fails to specify where the JFET region's width is measured, which varies due to the curvature of the p-well boundaries. (Def.'s Opening Claim Construction Br. (Doc. 104) at 23–24.) As a result, Defendant argues Claim Term A is indefinite, regardless of whether the JFET region is defined between the source regions or the p-wells. (Id.) Defendant contends that a given MOSFET device may fall within or outside the scope of the '633 Patent depending on where the JFET region's width is measured, creating an ambiguity rendering Claim Term A indefinite. (Id. at 24, 26.)

Plaintiff refutes this argument, explaining that "the JFET region should be measured at the narrowest point to achieve the intended design." (Pl.'s Responsive Claim Construction Br. (Doc. 117) at 9.) Plaintiff contends a person of skill in the art would know there is an optimum width that furthers the MOSFET device's design goal of "achiev[ing] the lowest possible on-resistance while meeting the desired blocking voltage specification." (Id. (quoting Ex. 2, Expert Report of Stanley Shanfield, Ph.D. ("Shanfield Report") (Doc. 103-2) at 17-18).)

The lack of measurement guidance is concerning to this court. Terms B and C in Claims 9 and 10 include specific widths for the JFET region. ('633 Patent (Doc. 83-1) at 11.) Additionally, the parties discuss the importance of the JFET region's width in designing and engineering a MOSFET device. (See, e.g., Def.'s Opening Claim Construction Br. (Doc. 104) at 29 ("Devices with different operating voltages and current characteristics will have different acceptable JFET widths. A higher operating voltage generally requires a wider JFET gap to account for the higher oxide fields that 'pinch' current flow through the device. On the other hand, low-current devices allow for a narrower JFET region, even at higher voltages, because on-state resistance is less of a design concern . . . .") (internal citations omitted); Pl.'s Opening Claim Construction

Br. (Doc. 103) at 27 ("'[A] JFET region that was too wide would result in the field across the gate oxide in the blocking state to exceed the electric field for the oxide breakdown, thus damaging the gate oxide[,]' and 'the device designed must ensure that the field in the oxide remains below a critical value to avoid early failure of the oxide.' Given these goals and reading these teachings, a skilled artisan would focus on keeping the JFET region widths as narrow as possible.") (quoting Shanfield Report (Doc. 103-2) at 17–18).) Accordingly, this court requests supplemental briefing to address: (1) whether the lack of measurement guidance renders Claim Term A indefinite; (2) whether the lack of measurement guidance renders the term "width" in Claim Terms B and C indefinite; and (3) any other position the parties may have on this issue.

This court's understanding is that a "JFET region is formed between . . . regions that 'pinch[]' current flow from source to drain." (Ex. 1, Expert Report of W. Allen Doolittle, Ph.D. Concerning Construction of Certain Terms in U.S. Patent No. 7,498,633 ("Doolittle Report") (Doc. 104-1) at 17.) The pinching action increases the device's resistance. (Id.) In contrast, a design goal for MOSFET devices "is to achieve the lowest possible on-resistance while meeting the desired blocking voltage specification." (Shanfield Report (Doc. 103-2) at 17.)

"One technique to minimize the JFET component on-state resistance involve[s] widening the JFET region and thereby reducing the degree of pinching." (Doolittle Report (Doc. 104-1) at 18.) However, "[t]hat approach ha[s] drawbacks" because "it increase[s] the cell size of the device" and "compromise[s] blocking voltage." (Id.) Relatedly, "a JFET region that [is] too wide would result in the field across the gate oxide in the blocking state to exceed the electric field for oxide breakdown, thus damaging the gate oxide." (Shanfield Report (Doc. 103-2) at 17.) "[T]he field in the oxide [must] remain below a critical value to avoid early failure of the oxide during operation in the field. . . . [I]n practice[,] the oxide field must be kept below about 3 MV/cm." (Id.)

"[R]educing one component of on-state resistance might increase another," as "reducing . . . the JFET width might also reduce the channel length and thereby reduce the channel component of on-state resistance," which "could counteract the increase in JFET resistance." (Doolittle Report (Doc. 104-1) at 19.) Regardless, "there are a number of well-known design considerations and variables that influence the design of a JFET region." (Id.) In sum, the JFET region's width is directly correlated with the blocking voltage and inversely correlated with the device's on-state resistance. "[T]here is an optimum

width at which one achieves the lowest on-resistance without allowing the oxide field to exceed the electric field for oxide breakdown in the blocking state." (Shanfield Report (Doc. 103-2) at 18.) The '633 Patent claims MOSFET devices in which "the JFET region [has] a width less than about three micrometers" and devices in which "the JFET region has a width of about one micrometer." ('633 Patent (Doc. 83-1) at 11.)

Plaintiff argues that a POSITA would know the JFET region's width "should be measured at the narrowest point to achieve the intended design." (Pl.'s Responsive Claim Construction Br. (Doc. 117) at 9.) Plaintiff's expert, Dr. Shanfield, explains that a "JFET region that was too wide would result in the field across the gate oxide in the blocking state to exceed the electric field for oxide breakdown, thus damaging the gate oxide," while a "JFET region that was too narrow would increase the on-state resistance, contrary to the design goal." (Shanfield Report (Doc. 103-2) at 17–18.) However, Dr. Shanfield does not explicitly opine on where the JFET region should be measured, nor does he contemplate the possibility of the curvature of the p-wells, as Dr. Doolittle explains. The term "narrowest point" appears for the first time in Plaintiff's Responsive Claim Construction Brief. (Pl.'s Responsive Claim Construction Br. (Doc. 117) at 9.) Measuring the JFET region at its "narrowest

point" is not provided for in the '633 Patent, its specification, or Dr. Shanfield's report.

Dr. Doolittle presents what appears to be uncontradicted expert testimony on behalf of Defendant concerning the curvature of the p-wells that results in variation on where the JFET region's width is measured. (Doolittle Report (Doc. 104-1) at 30-31.) Although expert testimony is extrinsic evidence, it may be considered when the intrinsic evidence does not resolve ambiguity in a disputed claim term. Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1584 (Fed. Cir. 1996). "[E]xtrinsic evidence in general, and expert testimony in particular, may be used only to help the court come to the proper understanding of the claims; it may not be used to vary or contradict the claim language." Id. "Nor may it contradict the import of other parts of the specification." Id. Here, however, Dr. Doolittle opines that "the claims and specification of the '633 Patent . . . fail to specify where along the boundary of the JFET region the claimed width measurement should be taken." (Doolittle Report (Doc. 104-1) at 29.) At most, in Figure 1, notation 36 illustrates the width of the JFET region. ('633 Patent (Doc. 83-1) at 2; id. at 9 ("the shorter width 36 of the JFET region"); id. ("As such, the design process of the

semiconductor device 10 may include a number of reiterative steps of selecting a width 36 . . . for the JFET region").)

Dr. Doolittle explains that the p-wells have "a generally curved profile." (Doolittle Report (Doc. 104-1) at 30.) Figure 1 shows curvature along the JFET region. ('633 Patent (Doc. 83-1) at 2.) Given this curvature, Dr. Doolittle continues:

> the choice of measurement location is meaningful in terms of determining whether a given MOSFET device falls within the scope of the claims. For example, . . . if the JFET region is defined between the lower portion of the p wells, then the region has a width of 4 micrometers and falls outside the scope of claim 9. If the JFET region is defined between [the] upper portion of the p wells, then the region has a width of 2.9 micrometers and falls within the scope of the claim.

(Doolittle Report (Doc. 104-1) at 31.) "The patent is silent about whether [the curved] portions [of the p-wells] should be included in the width measurement of the JFET region." (Id. at 32.) "The specification likewise identifies the width of the JFET region as item 36 in Figure 1 but does not explain how to measure the width relative to the non-uniform edges of the p wells." (Id.) Dr. Shanfield does not appear to address on behalf of Plaintiff how or where the JFET region's width should be measured. (See generally Shanfield Report (Doc. 103-2).) Accordingly, Dr. Doolittle's expert testimony does not appear to contradict or vary the '633 Patent or its specification, but only helps "the court come to a proper understanding of the claims."

Vitronics, 90 F.3d at 1584. Further, this court may rely upon an expert's uncontradicted testimony when reaching its conclusions, cf. Cordis Corp. v. Bos. Sci. Corp., 561 F.3d 1319, 1332 (Fed. Cir. 2009), although this court is not required to accept the expert's opinion, see Del Mar Avionics, Inc. v. Quinton Instrument Co., 836 F.2d 1320, 1325 (Fed. Cir. 1987).

"A claim is not indefinite if a person of skill in the art would know how to utilize a standard measurement method . . . to make the necessary measurement." Presidio Components, Inc. v. Am. Tech. Ceramics Corp., 875 F.3d 1369, 1376 (Fed. Cir. 2017). A "patent need not explicitly include information that is already well known in the art." Id. (citing Nautilus, Inc. v. Biosig Instruments, Inc., 572 U.S. 898, 906 (2014)). Even if there is no industry standard for a measurement, if the specification provides guidance on a certain measurement, that patent claim may be sufficiently definite. See id. (citing Ethicon Endo-Surgery, Inc. v. Covidien, Inc., 796 F.3d 1312, 1317–19 (Fed. Cir. 2015)).

In Presidio Components, Inc., the claim at issue for indefiniteness concerned multilayer capacitors with a fringe-effect capacitance between external contacts that [were] 'capable of being determined by measurement in terms of a standard unit.'" Id. at 1375 (quoting U.S. Patent No. 6,816,356). The patent and specification discussed using insertion loss

testing as a method for measuring capacitance; however, this method was "not well known as a method to measure the comparative contributions from different capacitances within the multilayer capacitor," nor did "the patent specification describe how to apply the insertion loss method to determine the portion of the overall capacitance that is attributable to the fringe-effect capacitance." Id. at 1376. That is, insertion loss testing was discussed in the patent and specification, but it was not an industry-standard measurement technique for the specific context of the patent at issue. Id. The Federal Circuit found the claim term sufficiently definite because the patent referenced a methodology for performing the measurement and because "the general approach of making modifications to a capacitor to isolate the impact of discrete capacitances was within the knowledge of someone skilled in the art." Id. at 1377. The Federal Circuit further explained:

> the claims do not require that fringe-effect capacitance exist at any particular level; they only require that it be capable of measurement in terms of a standard unit. To be sure, even where the claims require a particular test result, there may be (and often are) disputes between the parties as to the proper application of the test methodology in the circumstances of an individual case. But those disputes are disputes about whether there is infringement, not disputes about whether the patent claims are indefinite. Here, the general approach was sufficiently well established in the art and referenced in the patent to render the claims not indefinite. The claims

> do not rely on the unpredictable vagaries of any one person's opinion.

Id. (internal quotation marks and citation omitted).

In contrast, in Saso Golf, Inc. v. Nike, Inc., the Federal Circuit affirmed a district court's finding that a claim term concerning the precise boundaries of the toe and heel of a golf club was indefinite. 843 F. App'x 291, 295 (Fed. Cir. 2021). The district court made an underlying factual finding that "an artisan would not know the precise bounds of the toe and heel of a golf club." Id. at 294. This finding was based on expert testimony that persons of skill in the art "did not consider the terms 'toe' and 'heel' to have a single definition," and the patent or record failed to provide guidance on the measurement, so those persons "would not be able to choose a point related to the toe and heel from which to measure . . . ." Id. at 295. Consequently, the district court found the claim term indefinite. Id. The Federal Circuit affirmed both the district court's factual finding and its ultimate determination that the claim was indefinite. Id. at 295–96. The Federal Circuit also explained that only the defendant provided non-conclusory expert testimony concerning the issue of the toe and heel boundaries, whereas the plaintiff's expert did not provide testimony on this issue. Id.

The '633 Patent, unlike the patent at issue in Presidio Components, requires the JFET width to "exist at [a] particular

level," as specified in Claim Terms B and C. See 875 F.3d at 1376. Neither the '633 Patent, nor its specification, provides guidance on where the JFET region's width should be measured. Although Plaintiff's attorneys argue that the JFET region should be measured at its "narrowest point," (Pl.'s Responsive Claim Construction Br. (Doc. 117) at 9), this information is nowhere in the '633 Patent itself. Plaintiff's expert also does not provide any basis upon which to conclude that there is a "standard measurement method," see Presidio Components, 875 F.3d at 1376, or guidance within the specification, see Ethicon Endo-Surgery, 796 F.3d at 1317–19. Further, like in Saso Golf, Defendant has provided uncontradicted expert testimony that a person skilled in the art would not know where along the JFET region its width should be measured, while Plaintiff's expert has not addressed this issue. See 843 F. App'x at 295–96.

It appears to this court that the '633 Patent mandates certain widths for the JFET region, but this court is concerned with the issues raised herein. As a result of the foregoing, the issue of whether "the patent . . . fail[s] to inform, with reasonable certainty, those skilled in the art about the scope of the invention" because of variation in the JFET region's width measurement due to curvature in the p-wells may impact which

MOSFET devices fall within the scope of the '633 Patent and which do not. See Nautilus, 572 U.S. at 901.

The parties discuss this issue relative to Claim Term A, which explains the JFET region is "defined between the first source region and the second source region." ('633 Patent (Doc. 83-1) at 11.) However, Dr. Doolittle opines that "[t]his issue is present regardless of whether the JFET region is defined between the source regions or the p well regions." (Doolittle Report (Doc. 104-1) at 29.) This court is concerned that this issue may impact the construction of the word "width" in Claim Terms B and C, not Claim Term A. To resolve this concern, this court requests supplemental briefing to address: (1) whether the lack of measurement guidance renders Claim Term A indefinite; (2) whether the lack of measurement guidance renders the term "width" in Claim Terms B and C indefinite; and (3) any other position the parties may have on this issue.

For the foregoing reasons, the parties are hereby **ORDERED** to file supplemental briefs of no more than 2,500 words on this discrete issue by August 11, 2023. No responsive briefs will be permitted.

IT IS SO ORDERED.

This the 7th day of August, 2023.

William L. Osteen, Jr.
United States District Judge